

SKU603 Ultra Wideband Module Datasheet

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1 General Description

The SKU603 module is based on DecaWave's DW1000 Ultra Wideband (UWB) transceiver IC and GD32F130G8U6 MCU. It integrates antenna, all RF circuitry, power management and clock circuitry in one module. In order to save the module consumption power when the module is in static status, the module has integrated a three-axis linear accelerometer. It can be used in 2-way ranging or TDOA location systems to locate assets to a precision of 10 cm and supports data rates of up to 6.8 Mbps.



Figure 1: SKU603 Top View

2 Applications

- ◆ Precision real time location systems(RTLS) using two-way ranging or TDOA schemes in a variety of markets.
- ◆ Location aware wireless sensor networks(WSN)

3 Features

- ◆ **CPU:GD32F130G8U6**
 - Core: ARM® Cortex® -M3 RISC core
 - 48MHz maximum frequency
 - Single-cycle multiplication and hardware division
 - 64 KB on-chip Flash memory
 - up to 8 KB SRAM memory
 - one 12-bit ADC
 - up to five general-purpose 16-bit timers, a general-purpose 32-bit timer
- ◆ **UWB Transceiver IC:DW1000**
 - IEEE 802.15.4-2011 UW compliant
 - Supports 4 RF bands from 3.5 GHz to 6.5 GHz

- Programmable transmitter output power
- Fully coherent receiver for maximum range
- Data rates of 110 kbps, 850 kbps, 6.8 Mbps
- Maximum packet length of 1023 bytes for high data throughput applications
- Integrated MAC support features Supports 2-way ranging and TDOA
- ◆ **Accelerometer: LIS2DH12**
 - Ultra-low power consumption down to 2uA
 - $\pm 2g/\pm 4g/\pm 8g/\pm 16g$ selectable full scales
 - “Sleep-to-wake” and “return-to-sleep ” functions
 - Motion detection
 - Free-fall detection
- ◆ **Communication Interfaces**
 - UP to 2 USARTs
 - I2C
 - Serial Wire JTAG Debug Port

4 Applications Block Diagram

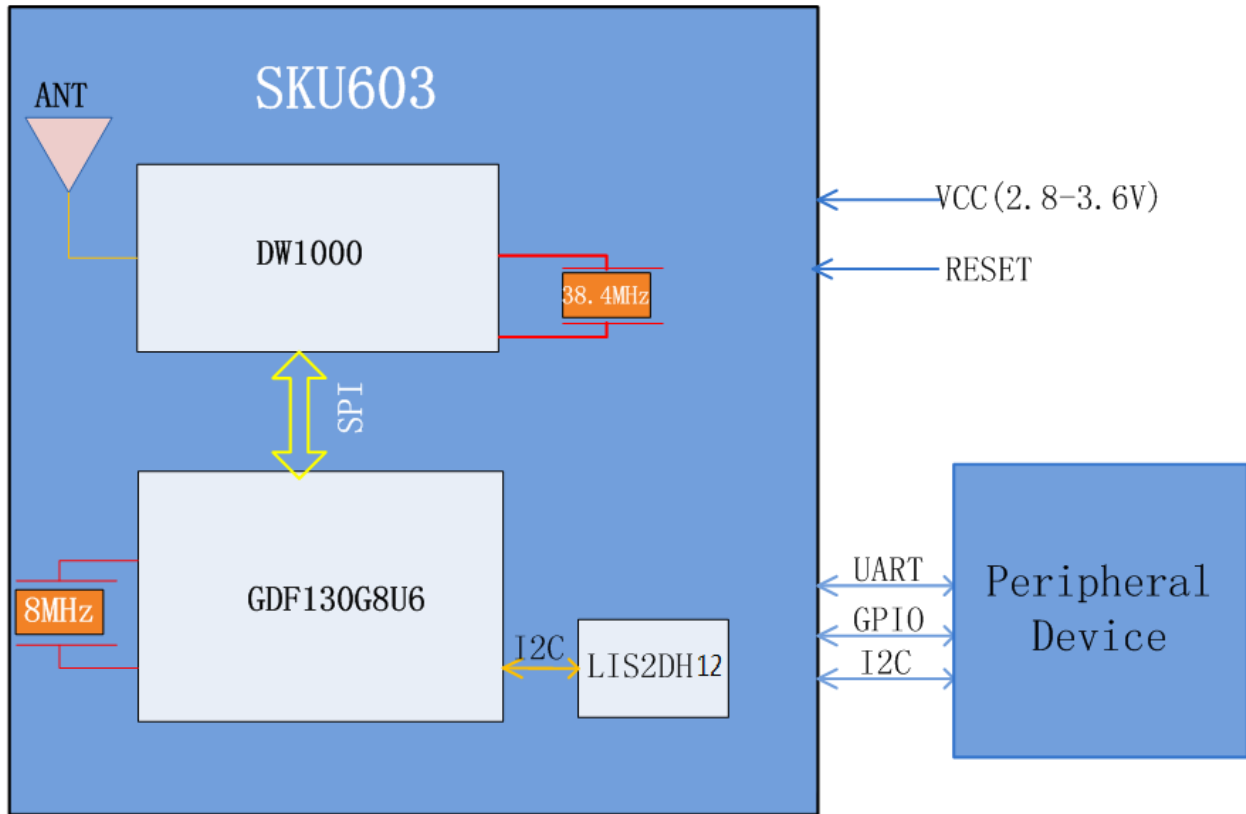


Figure 2: SKU603 Block Diagram

5 Module Specifications

Hardware Features	
Model	SKU603
Voltage	2.8V~3.6V
Dimension(L×W×H)	28.8×15.8×2.5 mm
Wireless Features	
Frequency Range	3244MHz---6999MHz
Channel Bandwidths	500MHz Channel 1, 2, 3 and 5
In-band blocking level	30 dBc
Out-of-band blocking level	55 dBc

Others	
Environment	Operating Temperature: -30°C~85°C
	Storage Temperature: -40°C~85°C
	Operating Humidity: 10%~90% Non-condensing
	Storage Humidity: 5%~90% Non-condensing

6 Module Pinout and Pin Description

6.1 Module Pinout

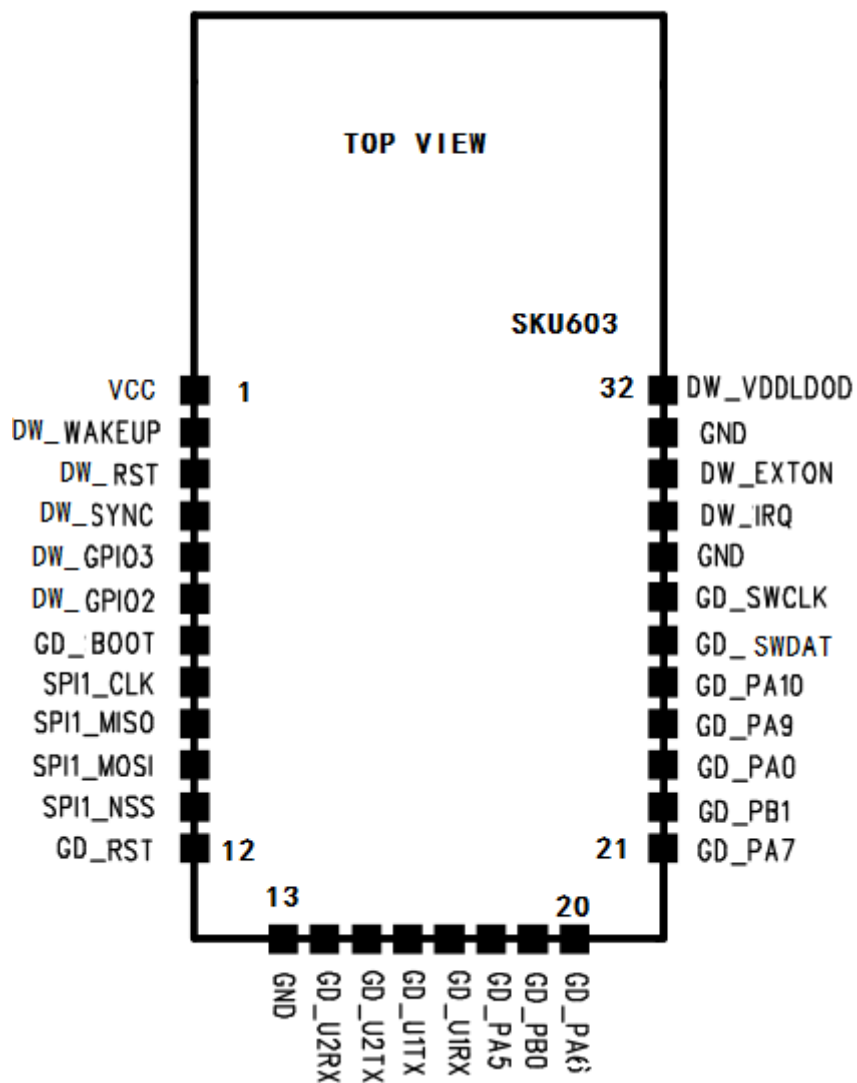


Figure 3: SKU603 Module Pinout

6.2 Pin Description

Pin No.	Pin Name	I/O	Description	Remark
1	VCC	P	Main Power Supply	2.8V to 3.6V
2	DW-WAKEUP	P	When asserted into its active high state, the WAKEUP pin brings the DW1000 out of SLEEP or DEEPSLEEP states into operational mode.	1.6V to 3.6V
3	DW-RST	DI	Reset pin. Active Low Output. May be pulled low by external open drain driver to reset the DW1000. Must not be pulled high by external source.	Connect to pin28 of GD32F130G8U6 in the module
4	DW_SYNC	DI	The SYNC input pin is used for external synchronization	Don't connect anything
5	DW_GPIO3	DI	It may be configured for use as a TXLED driving pin that can be used to light a LED following a transmission.	Connect to pin35 of GD32F130G8U6 in the module
6	DW-GPIO2	DI	General purpose I/O pin. It may be configured for use as a RXLED driving pin that can be used to light a LED during receive mode.	
7	GD_BOOT	DI	This pin can be used to set GD32F130G8U6 mode, which was pulled down in default	
8	SPI1_CLK	DIO	DW1000 SPI clock	Connect to GD32F130G8U6 SPI Interface in the module Don't connect anything for normal use.
9	SPI1_MISO	DIO	DW1000 SPI data output.	
10	SPI1_MOSI	DIO	SPI data input.	

11	SPI1_NSS	DIO	SPI chip select. .	
12	GD_RST	DI	This pin can be reset the whole module.	
13	GND	G	Ground	
14	GD_UART2RX	DIO	Default: USART2_TX,Alternate: USART1_TX ,PA2	Connect to pin9 of GD32F130G8U6 in the module
15	GD_UART2TX	DIO	Default:UART2_RX Alternate: USART1_RX ,PA3,ADC_IN3	Connect to pin8 of GD32F130G8U6 in the module
16	GD_UART1TX	DIO	Default: UART1TX,Alternate:PB6	Connect to pin27 of GD32F130G8U6 in the module
17	GD_UART1RX	DIO	USART1_RX,Alternate:PA5,USART2_RX ,PA15	Connect to pin23 of GD32F130G8U6 in the module
18	GD_PA5	DIO	Default: PA5 Alternate: SPI1_SCK, TM2_CH1_ETR Additional: ADC_IN5	Connect to pin11 of GD32F130G8U6 in the module
19	GD_PB0	DIO	Default: PB0 Alternate: TM3_CH3, TM1_CH2N, USART2_RX, EVENTOUT	Connect to pin14 of GD32F130G8U6 in the module
20	GD_PA6	DIO	Default: PA6 Alternate: SPI1_MISO, TM3_CH1, TM1_BKIN, TM16_CH1, EVENTOUT Additional: ADC_IN6	Connect to pin12 of GD32F130G8U7 in the module
21	GD_PA7	DIO	Default: PA7 Alternate: SPI1_MOSI, TM3_CH2, TM14_CH1, TM1_CH1N, TM17_CH1, EVENTOUT Additional: ADC_IN7	Connect to pin13 of GD32F130G8U8 in the module

22	GD_PB1	DIO	Default: PB1 Alternate: TM3_CH4, TM14_CH1, TM1_CH3N, SPI2_SCK	Connect to pin15 of GD32F130G8U9 in the module
23	GD_PA0	DIO	Default: PA0 Alternate: USART1_CTS (3) , USART2_CTS (4) , TM2_CH1_ETR, I2C2_SCL	Connect to pin6 of GD32F130G8U10 in the module
24	GD_PA9	DIO	Default: PA9 Alternate: USART1_TX, TM1_CH2, TM15_BKIN , I2C1_SCL	Connect to pin19 of GD32F130G8U11 in the module
25	GD_PA10	DIO	Default: PA10 Alternate: USART1_RX, TM1_CH3, TM17_BKIN, I2C1_SDA	Connect to pin20 of GD32F130G8U12 in the module
26	GD_SWDAT	DIO	Default: SWDAT Alternate: PA13	Debug Port
27	GD_SWCLK	DIO	Default: SWDAT Alternate: PA14	Debug Port
28	GND	G	Ground	
29	DW_IRQ	DI	Interrupt Request output from the DW1000 to the host processor. By default IRQ is an active-high output but may be configured to be active low if required. For correct operation in SLEEP and DEEPSLEEP modes it should be configured for active high operation. This pin will float in SLEEP and DEEPSLEEP states and may cause spurious interrupts unless pulled low.	The IRQ of DW1000 had connected to pin18 of GD32F130G8U6 in the module. Don't connect anything
30	GD_EXTON	DO	Control internal DC-DC converters in the module	Don't connect anything
31	GND	G	Ground	

32	DW_VDDLDO	P	Supply for DW1000 digital in the moudle ,which had already connected to a 1.8 DC-DC converter .	Don't connect anything
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- (1) P:Power supply
- (2) DI:Default Input
- (3) DO:Default Output
- (4) DIO:Default Input/Output
- (5) G:Ground

7 Interfaces

7.1 Power Supply

Regulated power for the SKU603 is required. The input voltage Vcc range should be 2.7V to 3.6V. Suitable decoupling must be provided by external decoupling circuitry (47uF and 0.1uF). It can reduce the noise from power supply and increase power stability.

7.2 System Function Interfaces

7.2.1 GPIOs

For SKU603 ,There are up to 14 general purpose I/O pins form GD32F130G8U6.Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI).The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output(push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

7.2.2 USART

For SKU603 ,There are up to 2 USARTs form GD32F130G8U6.The USART (USART1, USART2) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using

synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

7.2.3 Analog to digital converter (ADC)

(1) 12-bit SAR ADC engine with up to 1 MSPS conversion rate

(2) Conversion range: VSSA to VDDA (2.6 to 3.6 V)

(3) Temperature sensor

One 12-bit 1us multi-channel ADC is integrated in the device. It is a total of up to 16 multiplexed external channels and 3 internal channels for temperature sensor, voltage reference, VBAT voltage measurement. The conversion range is between $2.6\text{ V} < V_{DDA} < 3.6\text{V}$. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced usages. The ADC can be triggered from the events generated by the general-purpose timers (TMx) and the advanced-control timers (TM1) with internal connection.

The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value. Each device is factory-calibrated to improve the accuracy and the calibration data are stored in the system memory area.

8 Reference schematics

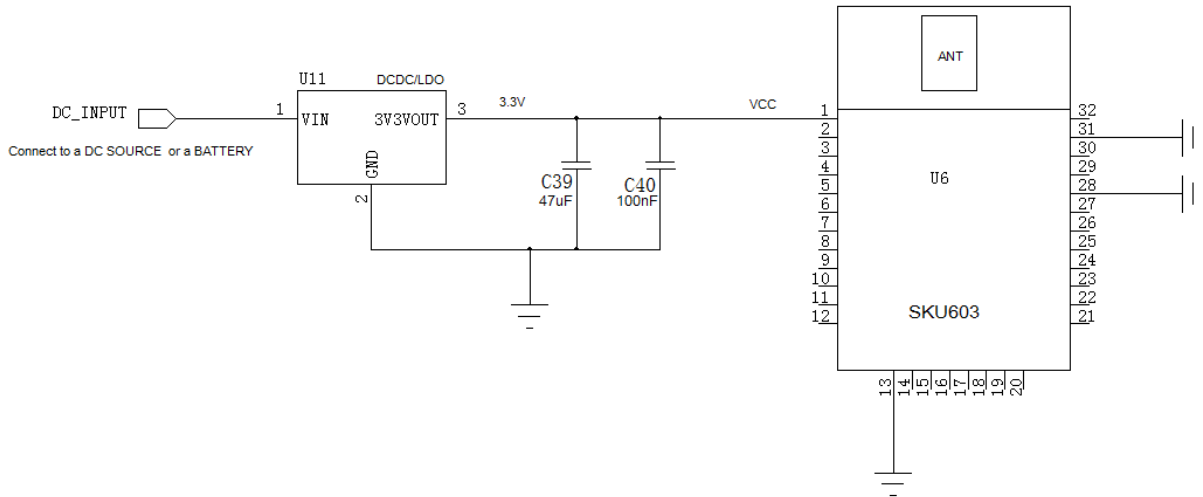


Figure 4: SKU603 reference schematics

The SKU603 supports the use of external switching regulators to reduce overall power consumption from the power source. Using switching regulators can reduce system power consumption. The EXTON pin can be used to further reduce power by disabling the external regulator when the DW1000 is in the SLEEP or DEEPSLEEP states (provided the EXTON turn on time is sufficient).

9 PCB Design Guide

When designing the PCB onto which SKU603 will be soldered, the proximity of the SKU603 on-board ceramic monopole antenna to metal and other non-RF transparent materials needs to be considered carefully. Two suggested placement schemes are shown below. In the areas marked “Keep-Out Area” there should be no metal either side, above or below (e.g. do not place battery under antenna). The placement schemes in Figure 6 show an application board with no non-RF transparent material in the keep-out area, or an application board with the antenna projecting off of the board so that the keep out area is in free-space. In this second scheme it is still important not to place metal components above or below the antenna in a system implementation.

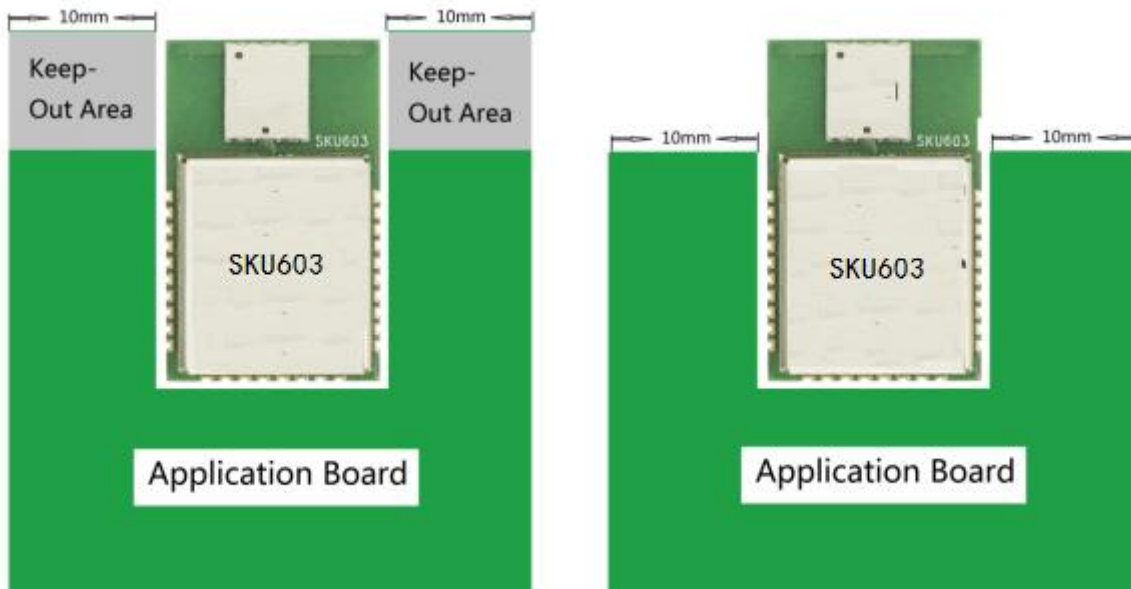


Figure 5: SKU603 Typical Lead-free Soldering Profile

10 PCB Footprint and Dimensions

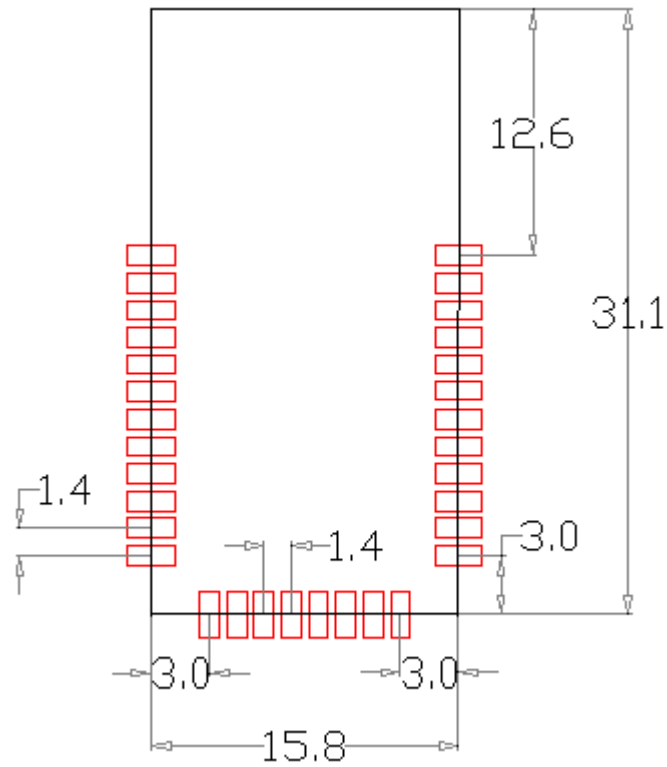


Figure 6: SKU603 PCB Footprint and Dimensions

11 Manufacturing Process Recommendations

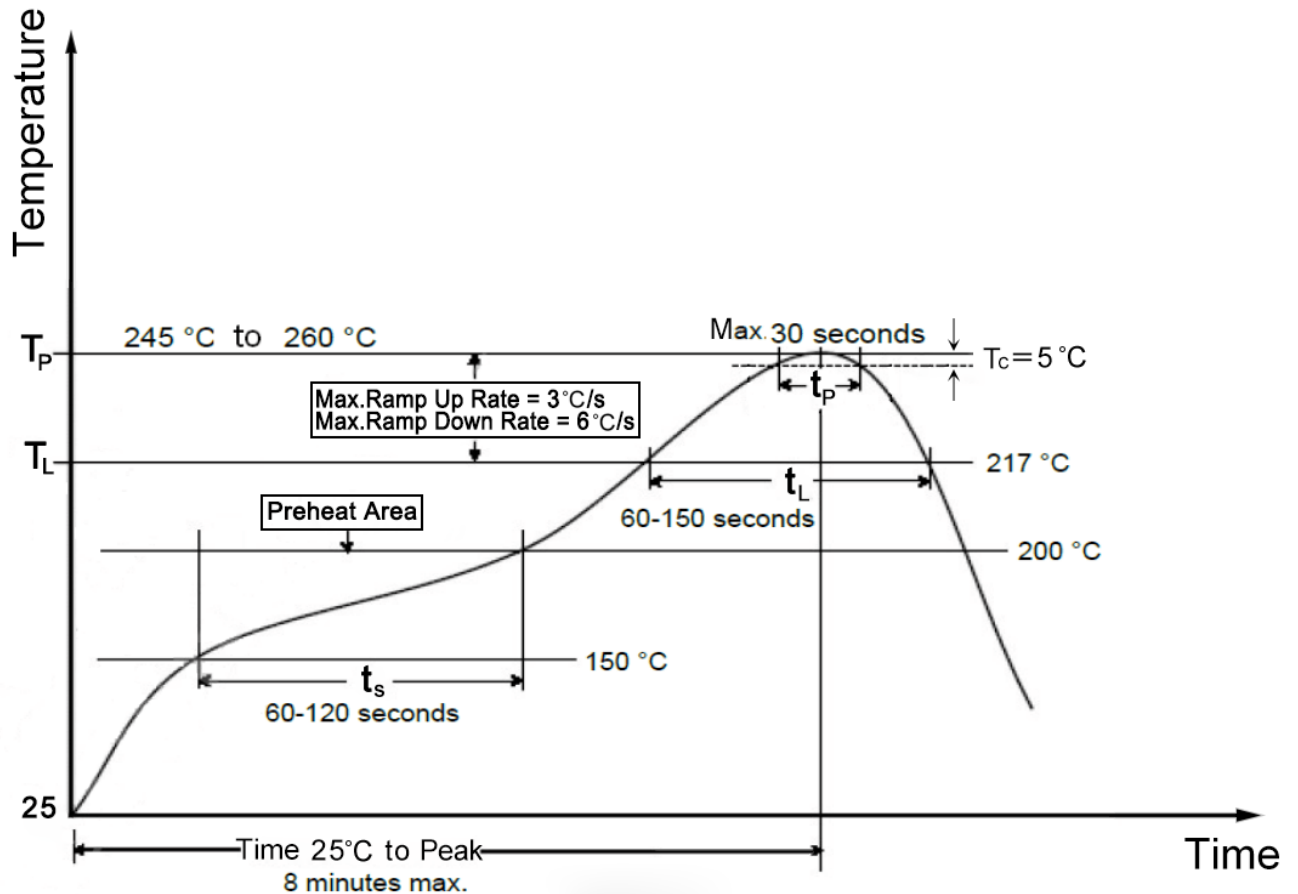


Figure7: SKU603 Typical Lead-free Soldering Profile

Note: The final re-flow soldering temperature map chosen at the factory depends on additional external factors, for example, choice of soldering paste, size, thickness and properties of the module's baseboard etc. Exceeding the maximum soldering temperature in the recommended soldering profile may permanently damage the module.

12 Packaging Specification

SKU603 modules are put into tray and 528 units per tray. Each tray is 'dry' and vacuum packaging.

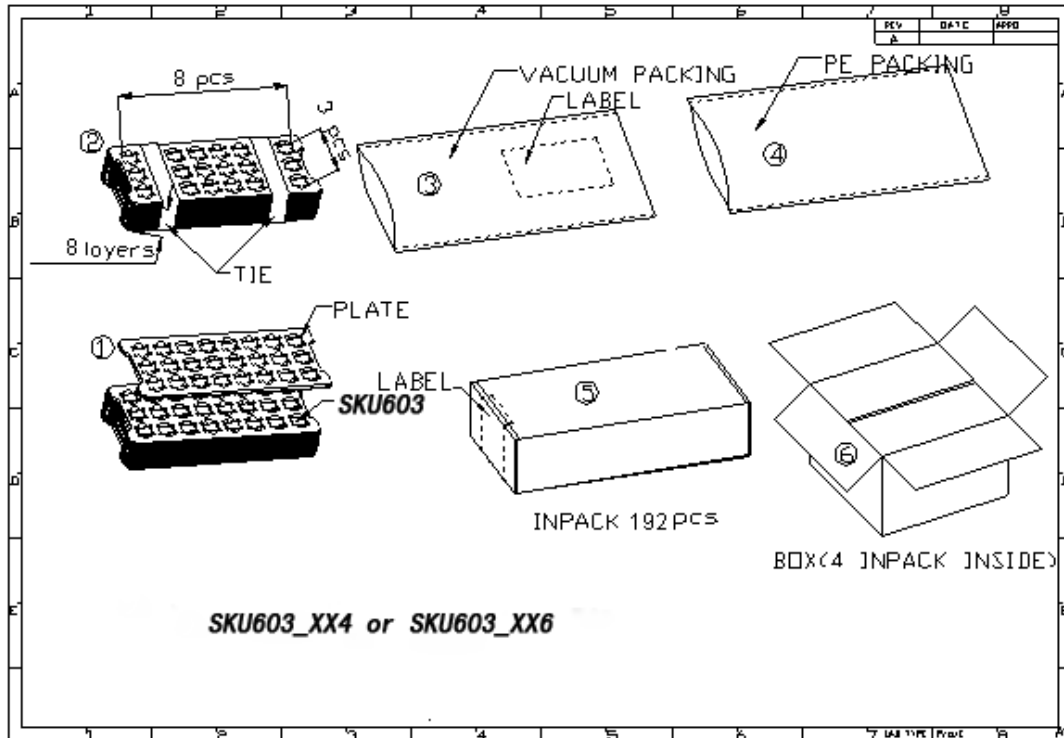


Figure 8: SKU603 Packaging

SKU603 series modules are Electrostatic Sensitive Devices and require special precautions while handling.



ESD precautions

The SKU603 modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling the SKU603 modules without proper ESD protection may destroy or damage them permanently.

The SKU603 modules are electrostatic sensitive devices (ESD) and require special ESD precautions typically applied to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling, transportation and operation of any application that incorporates the SKU603 module. Don't touch the module by hand or solder with non-anti-static soldering iron to avoid damage to the module.

13 Contact Information

Skylab M&C Technology Co., Ltd.

深圳市天工测控技术有限公司

Address: 6 Floor, No.9 Building, Lijincheng Scientific & Technical park, Gongye East Road,

Longhua District, Shenzhen, Guangdong, China

Phone: 86-755 8340 8210 (Sales Support)

Phone: 86-755 8340 8510 (Technical Support)

Fax: 86-755-8340 8560

E-Mail: technicalsupport@skylab.com.cn

Website: www.skylab.com.cn www.skylabmodule.com